A fully-integrated Bluetooth synthesizer using digital pre-distortion for PLL-based GFSK modulation

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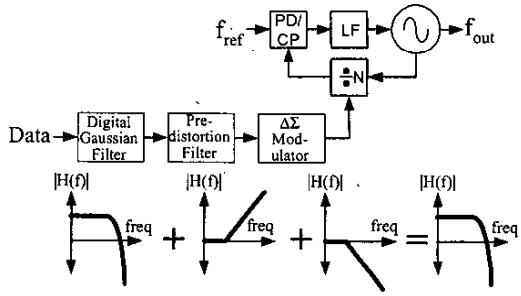
ABSTRACT — **Traditionally, GFSK modulation has been implemented using either I-Q up-conversion or by direct open-loop modulation of the VCO. The up-conversion approach is susceptible to an undesired image signal, and is costly in analog area and power. The open-loop modulation approach is prone to VCO frequency drift and gain errors. The approach described in this paper is a closed-loop modulation of a Delta-Sigma PLL with self-calibrated pre-distortion filtering. Prior examples of the pre-distortion approach have required either precision loop filter components or custom PLL response tuning. Our approach uses on-chip calibration algorithms which program digital filter coefficients to compensate for PLL loop gain and loop filter variations. This paper describes the fully integrated (including loop filter) 2.4 GHz Delta-Sigma frequency synthesizer, the digital pre-distortion filtering used to cancel the PLL's response, and the calibration algorithms used to adapt the pre-distortion filter coefficients. The synthesizer is implemented as part of a 0.25 µm CMOS Bluetooth radio, and uses approximately 35 mA on 4 mm² die area.**

I. Introduction

A Bluetooth radio can transmit or receive Gaussian Frequency Shift Keyed (GFSK) modulated data on one of 80 1-MHz channels spanning 2.402 – 2.480 GHz. Traditional approaches to GFSK data modulation have included I-Q up-conversion and open-loop modulation of the VCO. The work presented here uses closed loop PLL modulation with digital pre-distortion compensating for the PLL's closed-loop response to produce Bluetooth-compliant GFSK modulation [1,2,4].

The PLL compensation concept is shown in Fig. 1. A digital Gaussian filter performs the requisite data filtering for the Bluetooth standard. Due to noise considerations, it is difficult to implement a closed-loop PLL with a wide enough loop bandwidth to modulate data directly. The PLL implemented in this work has a loop bandwidth of 100 kHz. If left uncompensated, the response of this PLL would cause unwanted low-pass filtering of the Gaussian data. As shown in Fig. 1, the digital pre-distortion filter is inserted to the data signal path to cancel the PLL's response. The pre-distortion filter output combined with the channel information is Delta-Sigma modulated to generate a sequence of divide ratios for the PLL producing the desired GFSK waveform at the proper frequency channel. This work includes:

1) On-chip VCO 'Cap-select' tank tuning algorithm.
2) On-chip PLL loop gain estimation algorithm.
3) On-chip loop filter estimation.
4) Pre- distortion filter coefficient calculation based upon on-chip PLL loop gain and RC time constant estimation



II. Synthesizer Calibration and Settling

Bluetooth is a frequency hopping system; required receive-to-transmit turnaround time is 220 µs and the actual synthesizer settling time must be less than this when software and baseband overhead is considered. For this work, upon a frequency hop, there are 5 steps, which must be performed before the actual data transmission occurs.

1) VCO 'Cap Select' tank tuning Algorithm.
2) PLL loop gain estimation.
3) On-chip loop filter estimation.
4) Pre-distortion filter calculation.
5) PLL settling and data modulation.

The calibration process is performed each time that a frequency hop is done in order to account for:

1) Different VCO cap select settings over process, temperature and the Bluetooth frequency range.
2) Different VCO gains (and hence different PLL loop gains) over process, temperature and over the Bluetooth frequency range.

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3) Different loop filter component values over process and temperature.

For a given transmission the temperature variation will be small, so the VCO tank, cap select, gain calibration, and loop filter calibration are essentially static.

III. VCO TANK TUNING ALGORITHM

The VCO contains a bank of selectable capacitors [3,5], which allow the frequency to be coarsely set. The tank's 64 digital settings correspond to a range of about 500 MHz with about 8 MHz/step. Prior VCO tank tuning algorithms have included selecting tank setting by monitoring the VCO input voltage in an analog PLL [3], or by digitally based successive approximation register (SAR) algorithms. This work is based on digitally estimating the VCO frequency and selecting Cap Select settings based on these frequency estimates. The synthesizer is configured as a digital frequency-locked loop (DFLL), shown in Fig. 2. The VCO's frequency is estimated ($f_{ESTIMATE}$) and sampled upon every reference clock. The feedback path of the DFLL continuously adjusts the Cap Select setting of the VCO to maintain an average frequency equal to $f_{DESIRED}$ (a digital input corresponding to the channel frequency).

The VCO's analog input voltage is forced to a fixed common mode reference voltage, meaning that the VCO is in the center of its analog tuning range. The M counter is allowed to free-run while clocked by the prescaler output, and is resynchronized to the digital clock domain.

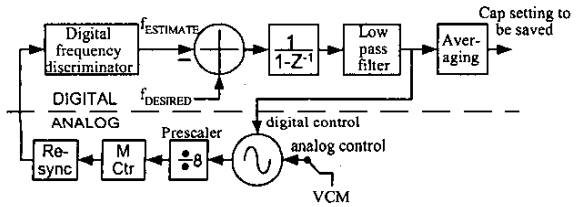

Fig. 2. Digital Frequency-Locked loop for 'cap select' coarse tuning algorithm.

The digital frequency estimate, $f_{ESTIMATE}$ is determined by taking the difference in M counter outputs between edges of the reference clock frequency, f_{REF} as follows. Since $f_{ESTIMATE}$ corresponds to the average number of prescaler output clocks (at a rate of $f_{VCO}/8$) during one reference clock cycle,

$$f_{ESTIMATE} = \frac{\frac{f_{VCO}}{8}}{f_{REF}} \qquad (1)$$

The feedback loop forces the average value of $f_{ESTIMATE}$ to the desired frequency $f_{DESIRED}$. A digital low-pass filter attenuates feedback variation due to frequency quantization noise, and the resulting cap select values are averaged to further reduce quantization noise. After time is allotted for DFLL loop settling, the average Cap Select value at the VCO is stored to be used for the remainder of the transmission .

IV. PLL CALIBRATION ALGORITHMS

A. Gain calibration algorithm.

The gain calibration approach presented in [4] implements a continuous automatic calibration. However, the frequent channel hopping in Bluetooth would make such an approach difficult due to the change in VCO gain upon each frequency hop. This work finds a 2-point straight-line approximation to the PLL open-loop gain upon each frequency hop. The Cap Select setting is fixed to the saved value, and the gain calibration algorithm is run to estimate the open loop unity gain bandwidth (ω_{LOOP}) of the PLL. This information is used to select a DAC setting for the PLL's Charge Pump (CP), and to calculate the pre-distortion filter coefficients. The gain calibration loop, shown in Fig. 3, is a DFLL similar to the cap select loop. By overriding the phase detector, the UP/DOWN signals to the CP and the 3-bit CP DAC value comprise a 4 bit sign+magnitude current-mode DAC. The VCO's analog input voltage is set by the CP DAC current into the loop filter resistor (loop filter capacitor C1 is shorted to VCM) which controls the VCO's frequency. The VCO's analog input voltage is equal to VCM + $DAC_{SETTING} I_{LSB} R_1$, where VCM is a common-mode voltage in the center of the VCO analog tuning range, $DAC_{SETTING}$ is the digital DAC input, I_{LSB} is the LSB size of the CP DAC, and R_1 is the loop filter resistor. On average, the output frequency will be:

$$f_{OUT} = f_0 + DAC_{SETTING}\left(I_{LSB} R_1 K_{VCO}\right), \qquad (2)$$

where f_0 is the VCO's output frequency with the analog input voltage at VCM for the saved Cap Select setting. The calibration algorithm steps are as follows:

1) Set desired frequency, $f_{DESIRED} = f_{CHAN} - \Delta f$, forcing average output frequency to $f_{CHAN} - \Delta f$, where f_{CHAN} is the channel frequency and Δf is a frequency value chosen to make a good 2-point linear approximation to the PLL loop gain.
2) After the loop settles, save average CP DAC input value as DAC_{NEG}. Thus,

$$f_{CHAN} - \Delta f = f_0 - DAC_{NEG}(I_{LSB} R_1 K_{VCO}) \quad (3)$$

3) Digitally set desired frequency, $f_{DESIRED} = f_{CHAN} + \Delta f$, forcing average output frequency to $f_{CHAN} + \Delta f$.

4) After the loop settles, save average CP DAC input value as DAC_{POS}. Thus,

$$f_{CHAN} + \Delta f = f_0 + DAC_{POS}(I_{LSB} R_1 K_{VCO}) \quad (4)$$

5) Calculate $\Delta DAC = DAC_{POS} - DAC_{NEG}$,

$$\Delta DAC = DAC_{POS} - DAC_{NEG} = \frac{2\Delta f}{I_{LSB} R_1 K_{VCO}} \quad (5)$$

6) The approximate unity gain bandwidth of the PLL is,

$$\omega_{LOOP} = \frac{I_P K_{VCO} R_1 C_1}{2\pi (C_1 + C_2) N} \quad (6)$$

7) Thus, from (5) and (6), given a desired loop gain $\omega_{LOOP\_DESIRED}$, a corresponding ideal DAC setting DAC_{IDEAL} can be determined as follows:

$$DAC_{IDEAL} = \frac{\Delta DAC \omega_{LOOP\_DESIRED} 2\pi (C_1 + C_2) N}{2\Delta f C_1} \quad (7)$$

8) Since only a 3-bit DAC is used, the calculated DAC_{IDEAL} value for a desired loop gain cannot be precisely set. Therefore, DAC_{IDEAL} is rounded down to DAC_{ACTUAL} which is the 3-bit DAC setting once the PLL is configured as a standard PLL. This allows a PLL loop gain close to desired loop gain.

9) The error between actual PLL loop gain (based on the actual 3-bit CP DAC) and ideal CP current is calculated. This error value is used to calculate compensation filter coefficients. Thus:

$$\omega_{LOOP\_ACTUAL} = \frac{DAC_{ACTUAL}}{DAC_{IDEAL}} \omega_{LOOP\_ACTUAL} \quad (8)$$

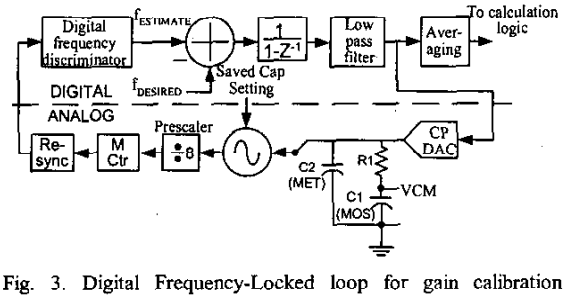

Fig. 3. Digital Frequency-Locked loop for gain calibration algorithm

B. RC tuner algorithm

An RC tune algorithm is run concurrently to the gain calibration algorithm (also used for an IF filter on this same IC). A separate RC tuner algorithm is run for the metal cap comprising the small loop filter cap, and for the MOS capacitor used for the large loop filter cap. Therefore, ω_{Z_ACTUAL} and ω_{P2_ACTUAL}, the actual values for ω_Z and ω_{P2} can be calculated and expressed as:

$$\omega_{Z\_ACTUAL} = \omega_{Z\_NOMINAL} \omega_{Z\_ERROR} \quad (9)$$

$$\omega_{P2\_ACTUAL} = \omega_{P2\_NOMINAL} \omega_{P2\_ERROR} \quad (10)$$

C. PLL settling

After the Cap Select and gain calibration algorithms are run, the synthesizer is configured as a standard PLL with the CP DAC set to DAC_{ACTUAL}. The PLL loop gain control reduces settling time and noise variation.

V. PREDISTORTION FILTERING

A. PLL linear model

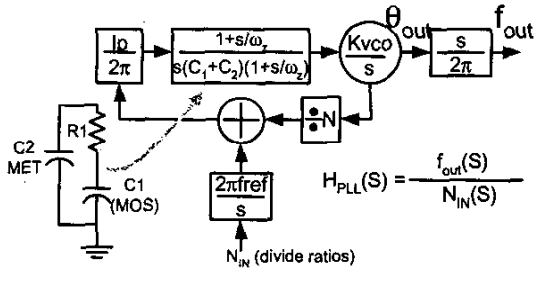

Fig. 4. PLL and ΔΣ modulator linear model

A linear model representing the PLL dynamics is shown in Fig. 4. From this model, it can be shown that $H_{PLL}(s)$, the transfer function from the ΔΣ modulator input to the output frequency is,

$$H_{PLL}(s) \cong \frac{f_{REF}(1 + \frac{s}{\omega_z})}{1 + \frac{s}{\omega_Z} + \frac{s^2}{\omega_{LOOP}\omega_Z} + \frac{s^3}{\omega_{P2}\omega_{LOOP}\omega_Z}}, \quad (11)$$

where ω_Z is the loop filter zero, ω_{P2} is the loop filter pole, and is the unity gain loop bandwidth of the PLL.

B. Pre-distortion filter

To compensate for the PLL's response in (11), the digital pre-distortion filter's frequency response must approximate the inverse of (11). By using the transform, $s \Leftrightarrow f_{REF}(1-Z^{-1})$ the transfer function of the desired pre-distortion filter is

$$H_{PRE}(Z) = \frac{1 + B_1(1-Z^{-1}) + B_2(1-Z^{-1})^2 + B_3(1-Z^{-1})^3}{1 + A_1(1-Z^{-1})} \quad (12)$$

where,

$$B_1 = \frac{f_{REF}}{\omega_z} \; B_2 = \frac{f_{REF}^2}{\omega_{LOOP}\omega_z} \; B_3 = \frac{f_{REF}^3}{\omega_{P2}\omega_{LOOP}\omega_z} \; A_1 = \frac{f_{REF}}{\omega_z}. \quad (13)$$

C. Filter coefficient calculation.

From the calculated values for ω_{LOOP_ACTUAL}, ω_{Z_ACTUAL}, and ω_{P2_ACTUAL}, (8,9,10) all of the coefficient values in (13) are calculated. The filter coefficients are updated during PLL settling, before data is being transmitted, to avoid transients in the digital filters.

VI. Results

The frequency synthesizer has been implemented in 0.25 µm CMOS. Output frequency during Cap Select and Gain Calibration is shown in Fig. 5. Modulation eye-diagram is shown in Fig. 6. As Table I shows, the synthesizer is in compliance with Bluetooth specifications.

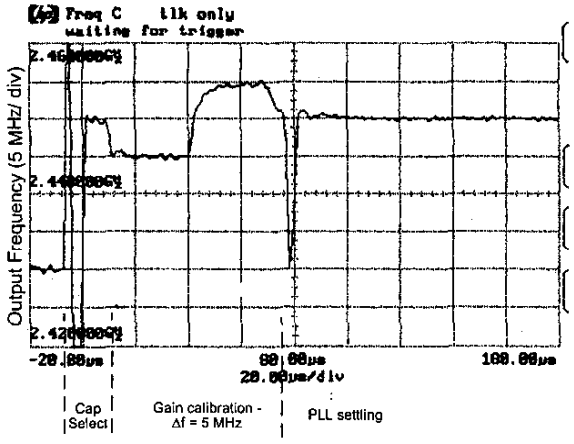

Fig. 5. Frequency domain plot showing cap select, gain calibration, and PLL settling (5 MHz/div).

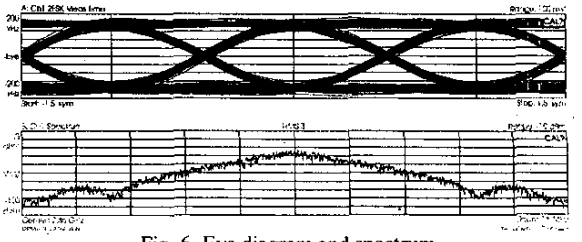

Fig. 6. Eye diagram and spectrum.

Table I: Performance summary:

Modulation index (11110000)	140 – 175 kHz
Modulation index (10101010)	> 115 kHz
Synthesizer area (analog)	1.5 mm^2
Synthesizer area (digital)	2.5 mm^2
Calibration + settling time	140 µs
Power dissipation	35 mA

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